What is claimed is:

1. A method for debugging a system-on-a chip (SoC), the SoC comprising system components to include at least one functional block, each of said blocks being controlled by a block clock and a clock control unit, the method comprising the steps of:

setting a breakpoint on a specific event occurring on the SoC;

monitoring events occurring on the SoC;

recognizing the occurrence of the specific event;

providing a debug trigger signal to each of said clock control units;

halting each block clock;

determining states of one or more of said system components; and,

utilizing said states to debug the SoC.

2. The method of claim 1 in which the specific event is an instruction that occurs within a functional block.

3. The method of claim 2 further comprising the step of generating a debug ready signal indicating to a user that the internal state of the SoC can be observed.

4. The method of claim 3 wherein at least one of said blocks comprises at least one scan chain, and said determining step comprises the steps of:

selecting from said at least one scan chain, a selected scan chain containing at least one register element;

configuring each of the at least one registers in said selected scan chain to contents required for scan mode;

providing control of the selected scan chain to a scan clock signal; and,

shifting out the contents of said at least one register element in the selected scan chain.

5. The method of claim 1 further comprising the steps of:

recognizing a debug clear signal triggered by the system environment and restoring operation of each block clock.

6. The method of claim 1 further comprising the steps of:

performing a single step execution of the SoC; and,

redetermining the states of said one or more of said system components.

7. The method of claim 1 further comprising the steps of:

performing an n-cycle step execution of the SoC where n is a positive integer; and,

redetermining the states of said one or more of said system components after execution of one or more of said n-cycle steps.

8. The method of claim 7 wherein at least one of said blocks comprises at least one scan chain, and said determining step comprises the steps of:

selecting from said at least one scan chain, a selected scan chain containing at least one register element;

configuring each of the at least one register elements in said selected scan chain to contents required for scan mode;

providing control of the scan chain to a scan clock signal; and,

shifting out the contents of the at least one register element in the selected scan chain.

9. The method of claim 1 further comprising the steps of:

setting an additional breakpoint on an additional specific event occurring on the SoC;

recognizing the occurrence of the additional specific event; and,

executing said providing, said halting, said determining and said utilizing steps only if a predetermined condition is met with respect to said specific event and said additional specific event.

10. The method of claim 1 further comprising the steps of:

performing an n-cycle step execution of only one block where n is a positive integer; and,

redetermining the states of said one or more of said system components after execution of one or more of said n-cycle steps.

11. An apparatus for debugging a system-on-a chip (SoC), the SoC comprising system components to include at least one functional block, each of said blocks being controlled by a block clock and a clock control unit, the apparatus comprising:

a first controller that recognizes a specific event occurring on the SoC;

a second controller that provides a debug trigger signal to each of said clock control units;

a third controller that halts each block clock upon detection of the presence of the debug trigger signal; and,

a circuit that outputs states of one or more of said system components;

wherein said states are utilized to debug the SoC.

12. The apparatus of claim 11 in which the specific event is an instruction that occurs within a functional block.

13. The apparatus of claim 12 further comprising a circuit that generates a debug ready signal indicating to a user that an internal state of the SoC can be observed.

14. The apparatus of claim 13 wherein at least one of said blocks comprises at least one scan chain, and said circuit that outputs states comprises:

a circuit that selects from said at least one scan chain, a selected scan chain containing at least one register element;

a circuit that configures each of the at least one register elements in said selected scan chain to contents required for scan mode;

a circuit that provides a scan clock signal to control the selected scan chain; and,

a circuit that shifts out the contents of said at least one register element in the selected scan chain.

15. The apparatus of claim 11 further comprising:

a circuit that recognizes a debug clear signal triggered by the system environment; and,

a circuit that restores operation of each block clock.

16. The apparatus of claim 11 further comprises a circuit that performs a single step execution of the SoC.

17. The apparatus of claim 11 further comprising:

a circuit that performs an n-cycle step execution of the SoC, where n is a positive integer; and,

said circuit that outputs states comprises a circuit that re-outputs the states of said one or more of said system components after execution of one or more of said n-cycle steps.

18. The apparatus of claim 17 wherein at least one of said blocks comprises at least one scan chain, and said circuit that outputs states further comprises:

a circuit that selects from said at least one scan chain, a selected scan chain containing at least one register element;

a circuit that configures each of the at least one register elements in said selected scan chain to contents required for scan mode;

a circuit that provides a scan clock signal to control the selected scan chain; and,

a circuit that shifs out the contents of said at least one register element in the selected scan chain.

19. The apparatus of claim 11 further comprising:

said first controller recognizes an additional specific event occurring on the SoC;

wherein only if a predetermined condition is met with respect to said specific event and said additional specific event, does the operation of each of said second controller, said third controller and said circuit that outputs states occur.

20. The apparatus of claim 11 further comprising:

a circuit that performs an n-cycle step execution of only one block, where n is a positive integer; and,

said circuit that outputs states comprises a circuit that re-outputs the states of said one or more of said system components after execution of one or more of said n-cycle steps.